



10GBASE-LR XFP Optical Transceiver **AXM752**

350 E. Plumeria Drive
San Jose, CA 95134-1911 USA
1-888-NETGEAR (638-4327)
E-mail: info@NETGEAR.com
www.NETGEAR.com

10GBASE-LR XFP Optical Transceiver



FEATURES

- Full duplex transmission at 9.95 to 11.08 Gbps
- 1310nm Electro Absorption Modulated Laser (EML) light source
- Standard LC duplex fiber-optic connector
- Compliant with IEEE 802.3ae Draft 5.0
- Compliant with XFP MSA Rev. 4.0
- I²C for integrated Digital Optical Monitoring
- Power consumption <2.5 W
- User friendly Plug-and-play style "Hot Swap"
- Small footprint which enables high board density
- XFI high speed I/O electrical interface
- Integrated signal conditioner to extend 200mm FR4 PCB trace signaling
- Temperature range 0°C - 70°C

Description

The AXM752 is a hot pluggable 10Gbps small-form-factor transceiver module integrated with the high performance un-cooled 1310nm EML-based transmitter, high sensitivity PIN receiver and signal conditioner for 10Gbps Ethernet applications that support link-distance up to 10km over standard SMF. It is compliant with the 10Gbps Ethernet IEEE 802.3ae standard and the INF-8077i XFP Multi-source Agreement (MSA).

The AXM752 is designed to be compliant with INF-8077i XFP Multi-source Agreement (MSA) with five digital monitoring functions: Temperature, Vcc, Tx optical power, TX laser bias current and RX received optical power.

Application

- 10G LAN switch
- 10G Ethernet switch/router
- 10G Fiber channel
- 10 Gigabit FC 10.5 Gb/s
- 10 Gigabit Ethernet 10.3 Gb/s

Performance

- AXM752 data link up to 10km in 9/125um single mode fiber.

1. Absolute Maximum Ratings

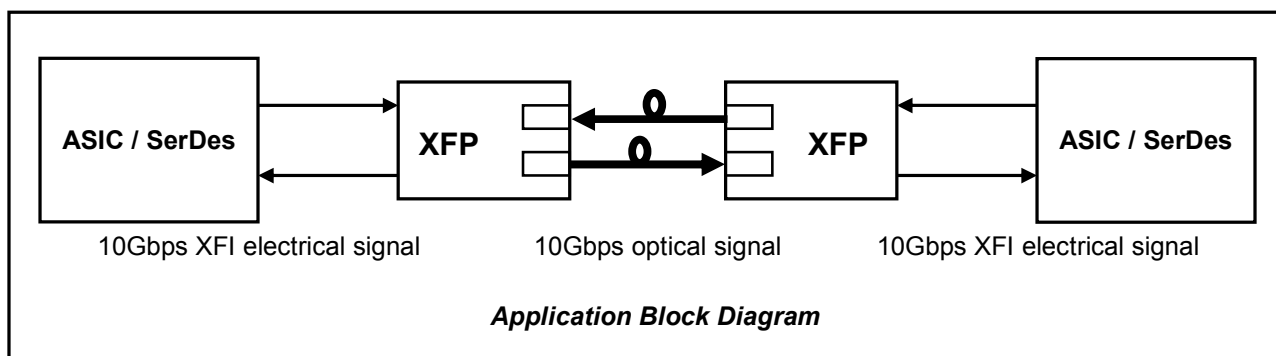
Parameter	Symbol	Min	Typ	Max	Units	Notes
Storage Temperature	T_S	-40		85	°C	
Storage Ambient Humidity	H_A	5		90	%	
+5V Power Supply	V_{CC5}	0		6.0	V	
+3.3V Power Supply	V_{CC3}	0		3.6	V	

2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Notes
Operating Case Temperature	T_C	0		70	°C	
Ambient Humidity	H_A	5		85	%	[1]
+3.3V Power Supply	V_{CC3}	3.135	3.3	3.465	V	
+5V Power Supply	V_{CC5}	4.75	5	5.25	V	
+3.3V Supply Current	I_{VCC3}		300	500	mA	
+5V Supply Current	I_{VCC5}		200	250	mA	
Total Power Dissipation	P_D		2.0	2.5	W	
Differential TX Data Input	$TD^+ - TD^-$	150	500	1000	mVp-p	[2,3]
Differential RX Data Output	$RD^+ - RD^-$	500	650	800	mVp-p	[4]

Notes:

1. Non-condensing
2. The data rate of input data is 10.3125Gb/s
3. Input voltage swing (differential) measured peak-to-peak
4. Output voltage swing (differential) measured peak-to-peak

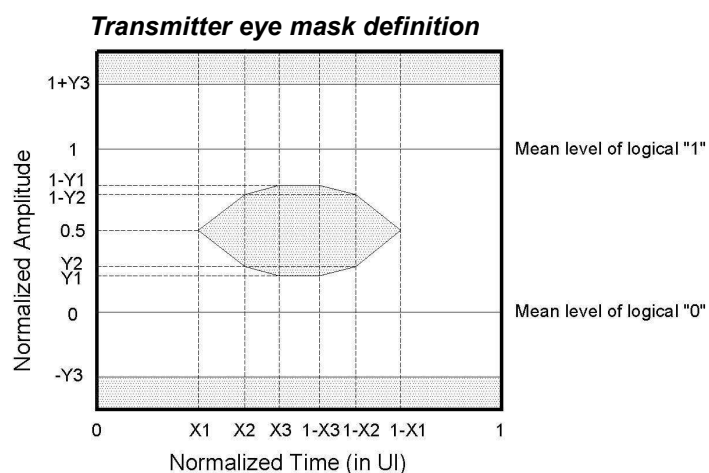


3. Optical Transmitter Characteristics ($T_c=0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Signaling speed (nominal)	R		10.3125		Gb/s	
Signaling speed variation from nominal				± 100	ppm	
Center Wavelength	λ	1260		1355	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Optical Modulation Amplitude	OMA	-5.2			dBm	
Extinction Ratio	ER	3.5			dB	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.40, 0.45, 0.25, 0.28, 0.40}				

Notes:

1. Even if the TDP < 1 dB, the OMA (min) must exceed this value.



4. Optical Receive Characteristics ($T_c=0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Signaling speed (nominal)	Ts		10.3125		Gb/s	
Signaling speed variation from nominal				± 100	ppm	
Center Wavelength	λ	1260		1355	nm	
Overload	P_o			0.5	dBm	
Receiver sensitivity in OMA	RSO			-12.6	dBm	[1]
LOS De-assert	LOS _D			-18	dBm	
LOS Assert	LOS _A	-30			dBm	

Notes:

1. Measured with test signal for BER = 10^{-12} .

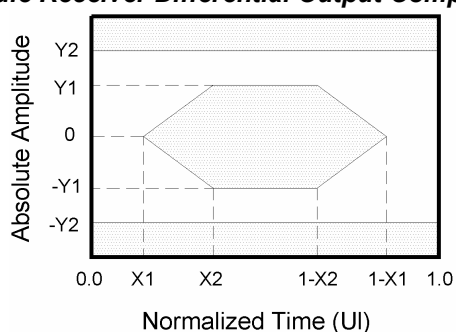
5. XFI Module Receiver Output Jitter Specifications at C'

Parameter – C'	Symbol	Min	Typ	Max	Units	Notes
Deterministic Jitter	DJ			0.18	UI (p-p)	[1]
Total Jitter	TJ			0.34	UI (p-p)	[1]
Eye Mask	X1			0.17	UI	
	X2			0.42	UI	
	Y1	170			mV	
	Y2			425	mV	

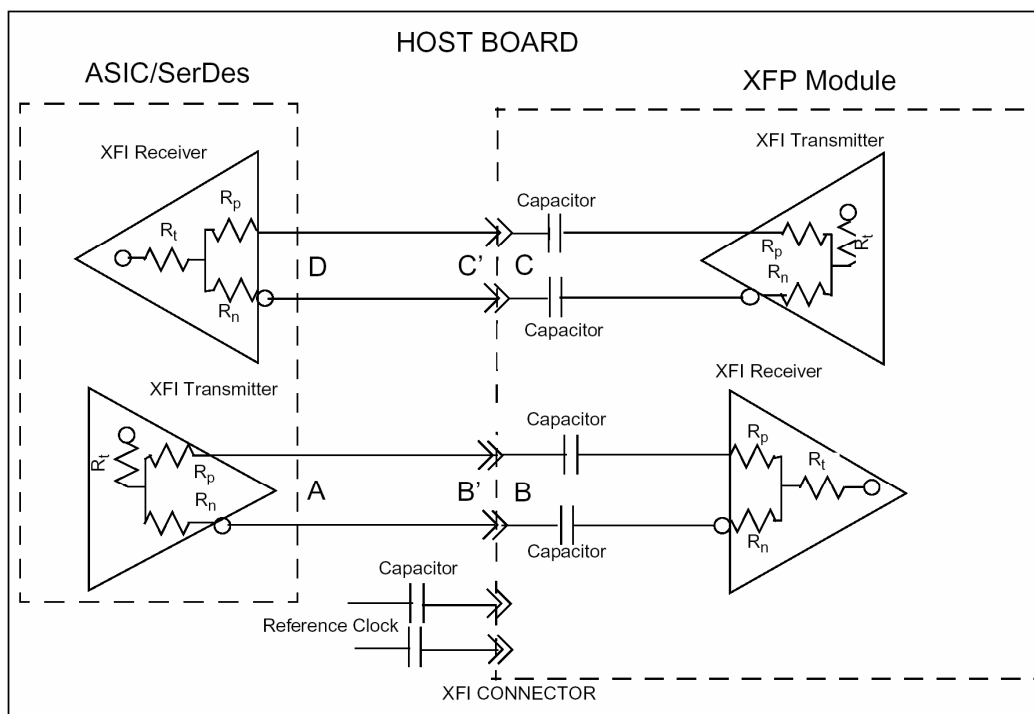
Notes:

- Includes jitter transferred from the optical receiver during any valid operational input condition.

XFI Module Receiver Differential Output Compliance Mask

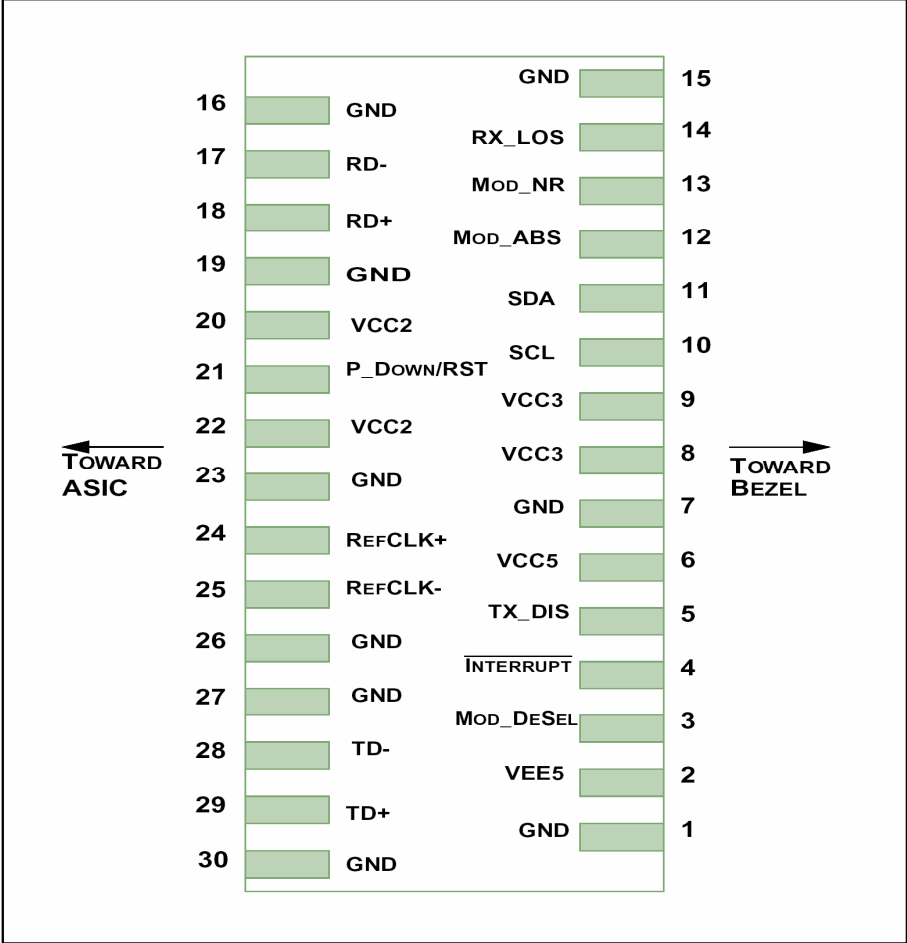


XFI Termination and AC Coupling

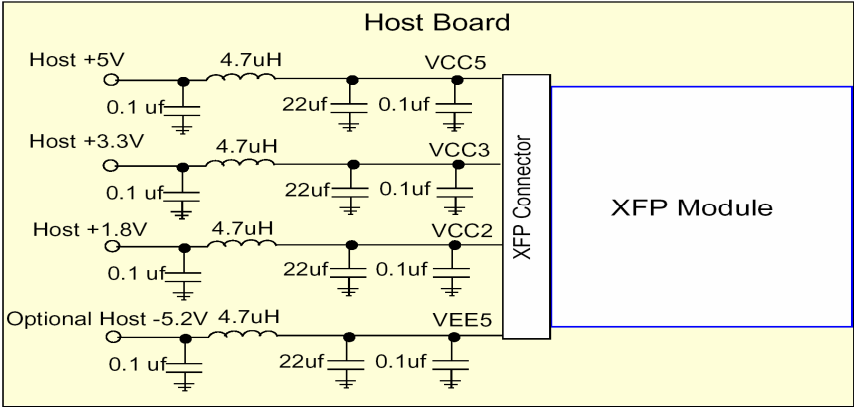


6. Pin Description

XFP Host Board Connector Pad Layout (Top View)



Recommended Host Board Supply Filtering Network



Module Electrical Pin Function Definition

Pin	Logic	Symbol	Name/Description	Note
1		GND	Module Ground	
2		VEE5	Optional -5.2V Power Supply --Not Required	
3	LVTTL-I	Mod_DeSel	Module De-select; When held low allows module to respond to 2-wire serial interface	
4	LVTTL-O	Interrupt Bar	Interrupt Bar; Indicates presence of an important condition which can be read over the 2-wire serial interface	[1]
5	LVTTL-I	TX_DIS	Transmitter Disable; Turns off transmitter laser output	
6		VCC5	+5V Power Supply	
7		GND	Module Ground	
8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	
10	LVTTL-I/O	SCL	2-Wire Serial Interface Clock	[1]
11	LVTTL-I/O	SDA	2-Wire Serial Interface Data Line	[1]
12	LVTTL-O	Mod_Abs	Indicates Module is not present. Grounded in the Module	[1]
13	LVTTL-O	Mod_NR	Module Not Ready; Indicating Module Operational Fault	[1]
14	LVTTL-O	RX_LOS	Receiver Loss Of Signal Indicator	[1]
15		GND	Module Ground	
16		GND	Module Ground	
17	CML-O	RD-	Receiver Inverted Data Output	
18	CML-O	RD+	Receiver Non-Inverted Data Output	
19		GND	Module Ground	
20		VCC2	+1.8V Power Supply --Not Required	
21	LVTTL-I	P_Down/RST	Power down; When high, requires the module to limit power consumption to 1.5W or below. 2-Wire serial interface must be functional in the low power mode.	
22		VCC2	+1.8V Power Supply --Not Required	
23		GND	Module Ground	
24	PECL-I	RefCLK-	Reference Clock Non-Inverted Input, AC coupled on the host board, Not required	
25	PECL-I	RefCLK+	Reference Clock Inverted Input, AC coupled on the host board, Not required	
26		GND	Module Ground	
27		GND	Module Ground	
28	CML-I	TD-	Transmitter Inverted Data Input	
29	CML-I	TD+	Transmitter Non-Inverted Data Input	
30		GND	Module Ground	

Notes:

1. Module ground pins Gnd are isolated from the module case and chassis ground within the module.
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.

7. Low Speed Electrical Hardware Pins

In addition to the 2-wire serial interface the XFP module has the following low speed pins for control and status:

- Mod_NR
- Mod_DeSel
- Interrupt
- TX_DIS
- Mod_ABS
- RX_Los
- P_Down/RST.

1 MOD_NR

The Mod_NR is an output pin that when High, indicates that the module has detected a condition that renders transmitter and or receiver data invalid, shall consist of logical OR of the following signals:

- Transmit Signal Conditioner Loss of Lock
- Transmitter Laser Fault
- Receiver Signal Conditioner Loss of Lock

2 MOD_DESEL

The Mod_DeSel is an input pin. When held Low by the host, the module responds to 2-wire serial communication commands. The Mod_DeSel allows the use of multiple XFP modules on a single 2-wire interface bus.

When the Mod_DeSel pin is “High” , the module shall not respond to or acknowledge any 2-wire interface communication from the host. Mod_DeSel pin must be pulled to VCC3 in the module.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the Mod_DeSel assert time after any XFP modules are deselected. Similarly, the host must wait at least for the period of the Mod_DeSel deassert time before communicating with the newly selected module. The assertion and de-assertion periods of different modules may overlap as long as the above timing requirements are met.

3 INTERRUPT

Interrupt is an output pin. When “Low” , indicates possible module operational fault or a status critical to the host system. The Interrupt pin is an open collector output and must be pulled up to Host_Vcc the host board.

4 TX_DIS

TX_DIS is an input pin. When TX_DIS is asserted High, the XFP module transmitter output must be turned off. The TX_DIS pin must be pulled up to VCC3 in the XFP module.

5 MOD_ABS

Mod_ABS is pulled up to Host_Vcc on the host board and grounded in the XFP module. Mod_ABS is then asserted “High” when the XFP module is physically absent from a host slot.

6 RX_LOS

The RX_LOS when High indicates insufficient optical power for reliable signal reception. The RX_LOS pin is an open collector output and must be pulled up to Host_Vcc on the host board.

7 P_DOWN/RST

This is a multifunction pin for module Power Down and Reset. The P_Down/RST pin must be pulled up to VCC3 in the XFP module.

7.1 POWER DOWN FUNCTION

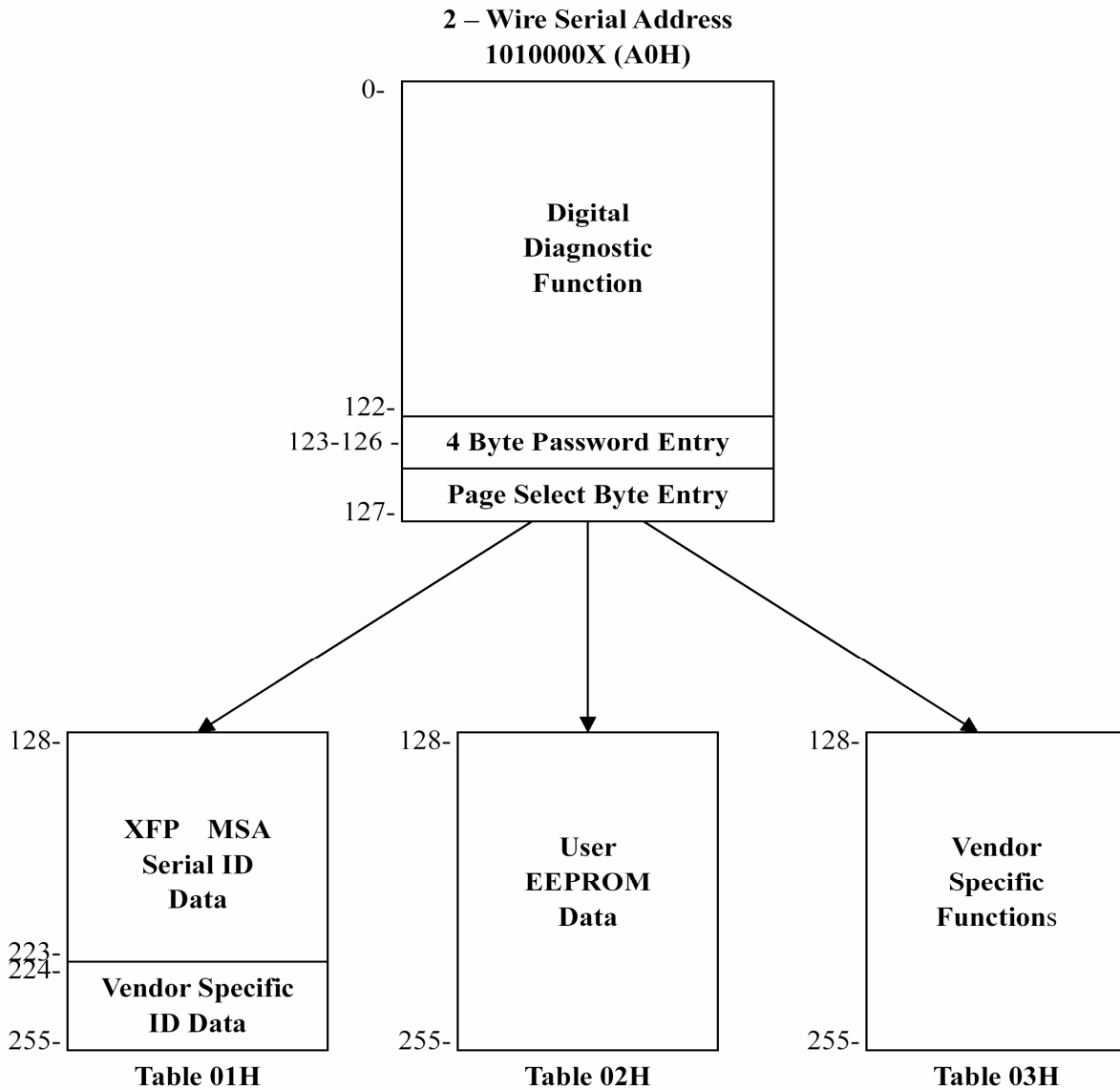
The P_Down pin, when held High by the host, places the module in the standby (Low Power) mode with a maximum power dissipation of 1.5W.

7.2 RESET FUNCTION

The negative edge of P_Down/RST signal initiates a complete module reset. Notes:

3. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.

8. Memory Map of Management Interface



The lower memory table (Byte 0~127) is for digital diagnostics and control functions. Besides, it has been allocated three upper memory tables for serial ID, user writable and vendor specific functions. The detail memory content is listed as following table.

9. EEPROM Serial ID Memory Contents (2-Wire Address A0h)

Address	Hex	ASCII	Address	Hex	ASCII	Address	Hex	ASCII
128	06		171	37	7	214	DC	
129	50		172	35	5	215	DC	
130	07		173	32	2	216	DC	
131	40		174	20		217	DC	
132	00		175	20		218	DC	
133	00		176	20		219	DC	
134	00		177	20		220	08	
135	00		178	20		221	60	
136	00		179	20		222	67	
137	00		180	20		223		Note 4
138	00		181	20		224	VS	Note 5
139	90		182	20		225	VS	
140	64		183	20		226	VS	
141	68		184	41		227	VS	
142	0A		185	20		228	VS	
143	00		186	66	3	229	VS	
144	00		187	58		230	VS	
145	00		188	0F		231	VS	
146	00		189	A0		232	VS	
147	60		190	46		233	VS	
148	4E	N	191		Note 1	234	VS	
149	45	E	192	7D		235	VS	
150	54	T	193	96		236	VS	
151	47	G	194	55		237	VS	
152	45	E	195	00		238	VS	
153	41	A	196	SN	Note 2	239	VS	
154	52	R	197	SN		240	VS	
155	20		198	SN		241	VS	
156	20		199	SN		242	VS	
157	20		200	SN		243	VS	
158	20		201	SN		244	VS	
159	20		202	SN		245	VS	
160	20		203	SN		246	VS	
161	20		204	SN		247	VS	
162	20		205	SN		248	VS	
163	20		206	SN		249	VS	
164	C1		207	SN		250	VS	
165	00		208	SN		251	VS	
166	06		209	SN		252	VS	
167	6E		210	SN		253	VS	
168	41	A	211	SN		254	VS	
169	58	X	212	DC	Note 3	255	VS	
170	4D	M	213	DC				

Notes:

- 1) CC_BASE : Check code for Base ID Fields (address 120~190)
- 2) Vendor SN (address 196~211)
- 3) Date Code (address 212~219)
- 4) CC_EXT : Check code for Extended ID Fields (address 192~222)
- 5) Address 224~255 is reserved for vendor specific EEPROM

10. Digital Diagnostic Monitoring Interface

Alarm and Warning Thresholds (2-Wire Address A0h)

Address	# Bytes	Name	Value (Dec.)	Unit
01	1	Signal Conditioner Control		
02–03	2	Temp High Alarm	90	
04–05	2	Temp Low Alarm	-10	
06–07	2	Temp High Warning	85	°C
08–09	2	Temp Low Warning	-5	
10–17	8	Reserved		
18–19	2	Bias High Alarm	lop+60 mA	
20–21	2	Bias Low Alarm	lop-25 mA	
22–23	2	Bias High Warning	lop+55 mA	mA
24–25	2	Bias Low Warning	lop-20 mA	
26–27	2	TX Power High Alarm	P+3	
28–29	2	TX Power Low Alarm	P-3	
30–31	2	TX Power High Warning	P+2	dBm
32–33	2	TX Power Low Warning	P-2	
34–35	2	RX Power High Alarm	-3	
36–37	2	RX Power Low Alarm	-23	
38–39	2	RX Power High Warning	-5	dBm
40–41	2	RX Power Low Warning	-21	
42–43	2	AUX 1 High Alarm	5.5	
44–45	2	AUX 1 Low Alarm	4.5	
46–47	2	AUX 1 High Warning	5.3	Volt
48–49	2	AUX 1 Low Warning	4.7	
50–51	2	AUX 2 High Alarm	3.6	
52–53	2	AUX 2 Low Alarm	3.0	
54–55	2	AUX 2 High Warning	3.5	Volt
56–57	2	AUX 2 Low Warning	3.1	
96	1	Temperature MSB		
97	1	Temperature LSB		
98–99	10	Reserved		
100	1	TX Bias MSB		
101	1	TX Bias LSB		
102	1	TX Power MSB		
103	1	TX Power LSB		
104	1	RX Power MSB		
105	1	RX Power LSB		
106	1	AUX 1 MSB(5V)		
107	1	AUX 1 LSB (5V)		
108	1	AUX 2 LSB (3.3V)		
109	1	AUX 2 LSB (3.3V)		

Notes:

- 1) P: Operating optical power of transmitter at room temperature
- 2) lop: Operating bias current of transmitter at room temperature

General State/ Control Bits

Byte	Bit	Name	Description
1	0	Signal Conditioner Control	Default value of this bit is 0
1	1	XFI Loopback	XFI loopback enable when this bit set to 1
1	2	Lineside Loopback	Not Implement
1	4-7	Data Rate Control	Default setting is 10.3Gbps
110	7	Tx Disable State	Digital state of the Tx disable input pin
110	6	Optional Soft TX Disable	Read/ Write bit that allow software disable of laser
110	5	MOD_NR State	Digital state of Module Not Ready
110	4	P-Down State	Digital state Power Down
110	3	Soft P_Down	Software Power Down
110	2	Interrupt	Interrupt Bar State
110	1	LOS	Digital state of the LOS output pin.
110	0	Data_Not_Ready	Digital state of Data_Not_Ready
111	7	TX_NR State	Digital state of Tx Not Ready State
111	6	TX_Fault State	Digital state of Tx Fault State
111	5	TX_CDR not Locked	Digital state of Tx CDR not Locked
111	4	RX_NR State	Digital state of Rx Not Ready
111	3	RX_CDR not Locked	Digital state of Rx CDR not Locked
119-122	All	New Password Entry	Location for Entry of New Optional Password
123-126	All	Password Entry	Location for Entry of Optional Password
127	All	Table Select	Entry Location for Table Select Byte

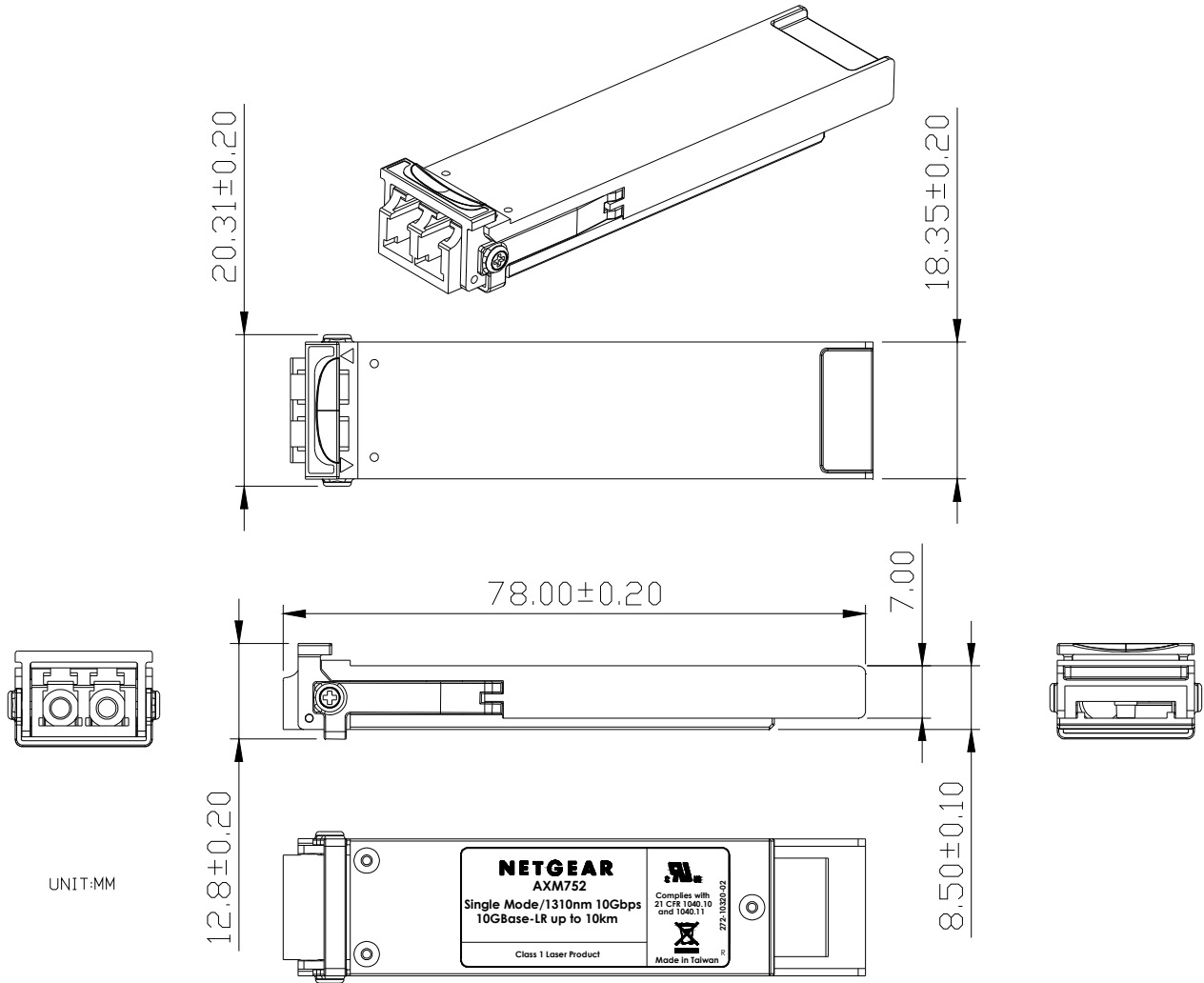
Optional Set of Alarm and Warning

Byte	Bit	Name	Description
80	7	Temp High Alarm	Set when internal temperature exceeds high alarm level
80	6	Temp Low Alarm	Set when internal temperature is below low alarm level
80	5	Reserved	
80	4	Reserved	
80	3	Tx Bias High Alarm	Set when Tx Bias current exceeds high alarm level
80	2	Tx Bias Low Alarm	Set when Tx Bias current is below low alarm level
80	1	Tx Power High Alarm	Set when Tx output power exceeds high alarm level
80	0	Tx Power Low Alarm	Set when Tx output power is below low alarm level
81	7	Rx Power High Alarm	Set when received power exceeds high alarm level
81	6	Rx Power Low Alarm	Set when received power is below low alarm level
81	5	AUX1 High Alarm	Set when internal 5V supply voltage exceeds high alarm level
81	4	AUX1 Low Alarm	Set when internal 5V supply voltage is below low alarm level
81	3	AUX2 High Alarm	Set when internal 3.3V supply voltage exceeds high alarm level
81	2	AUX2 Low Alarm	Set when internal 3.3V supply voltage is below low alarm level
81	1	Reserved	
81	0	Reserved	
82	7	Temp High Warning	Set when internal temperature exceeds high warning level
82	6	Temp Low Warning	Set when internal temperature is below low warning level
82	5	Reserved	
82	4	Reserved	
82	3	Tx Bias High Warning	Set when Tx Bias current exceeds high warning level
82	2	Tx Bias Low Warning	Set when Tx Bias current is below low warning level
82	1	Tx Power High Warning	Set when Tx output power exceeds high warning level
82	0	Tx Power Low Warning	Set when Tx output power is below low warning level

83	7	Rx Power High Warning	Set when received power exceeds high warning level
83	6	Rx Power Low Warning	Set when received power is below low warning level
83	5	AUX1 High Warning	Set when internal 5V supply voltage exceeds high warning level
83	4	AUX1 Low Warning	Set when internal 5V supply voltage is below low warning level
83	3	AUX2 High Warning	Set when internal 3.3V supply voltage exceeds high warning level
83	2	AUX2 Low Warning	Set when internal 3.3V supply voltage is below low warning level
83	1	Reserved	
83	0	Reserved	

11. Mechanical Outline Dimensions

Transmitter Wavelength / Application	Latch Color Identifier
1310nm / LR	 Blue



11. Regulatory Compliance

Feature	Reference	Performance
Electromagnetic Interference (EMI)	FCC CRF 47, Part15 Class B EN 55022 Class B (CISPR 22A)	(1) Satisfied with electrical characteristics of product spec. (2) No physical damage
Radio Frequency Electromagnetic Field	EN 61000-4-3 IEC 61000-4-3	
Electrostatic Discharge to the Duplex LC Receptacle	EN 61000-4-2 IEC 61000-4-2 IEC 801.2	
Electrostatic Discharge to the Electrical Pins	MIL-STD-883E Method 3015.7	
Eye Safety	US FDA CDRH AEL Class 1	
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment Including Electrical Business Equipment	UL File # E239394

Appendix A. Document Revision

Version No.	Date	Description
S0	2006-04-25	Preliminary datasheet for RoHS version
S1	2006-08-25	Update Digital Diagnostic Memory Map contents
S2	2007-10-02	Modify the dimension of label
0A	2007-11-09	Modify the Byte 165~167 of A0h

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